

## WHAT IS CLAIMED IS:

1           1.    A differential-to-single-ended (DSE) converter capable of  
2   receiving a positive differential input signal and a negative  
3   differential input signal and generating a single-ended output  
4   signal, said DSE converter comprising:  
5                a first comparator having a non-inverting input coupled  
6   to said positive differential input signal and an inverting input  
7   coupled to said negative differential input signal;  
8                a second comparator having an inverting input coupled to  
9   said positive differential input signal and a non-inverting input  
10   coupled to said negative differential input signal;  
11               a first D flip-flop having an input connected to Logic 1  
12   and clocked by a rising edge on an output of said first comparator;  
13               a second D flip-flop having an input connected to Logic 1  
14   and clocked by a rising edge on an output of said second  
15   comparator; and  
16               a latch circuit having a first input coupled to an output  
17   of said first D flip-flop and a second input coupled to an output  
18   of said second D flip-flop, wherein a rising edge on an output of  
19   said first D flip-flop causes an output of said latch to change  
20   state and a rising edge on an output of said second D flip-flop  
21   causes said latch output to change state.

1           2.    The differential-to-single-ended (DSE) converter as set  
2    forth in Claim 1, wherein said latch circuit comprises a first NOR  
3    gate having a first input coupled to said output of said first D  
4    flip-flop, a second input, and an output.

1           3.    The differential-to-single-ended (DSE) converter as set  
2    forth in Claim 2, wherein said latch circuit comprises a second NOR  
3    gate having a first input coupled to said output of said second D  
4    flip-flop, a second input coupled to said first NOR gate output,  
5    and an output coupled to said second input of said first NOR gate.

1           4.    The differential-to-single-ended (DSE) converter as set  
2    forth in Claim 3, wherein said first NOR gate is coupled to said  
3    first D flip-flop output by a first OR gate having a first input  
4    coupled to said first D flip-flop output, a second input coupled to  
5    Logic 0, and an output coupled to said first input of said first  
6    NOR gate.

1           5.    The differential-to-single-ended (DSE) converter as set  
2    forth in Claim 4, wherein said first NOR gate output is coupled to  
3    a reset input of said first D flip-flop.

1           6.    The differential-to-single-ended (DSE) converter as set  
2   forth in Claim 5, wherein said first NOR gate output is coupled to  
3   said reset input of said first D flip-flop via a buffer circuit.

1           7.    The differential-to-single-ended (DSE) converter as set  
2   forth in Claim 4, wherein said second NOR gate output is coupled to  
3   a reset input of said second D flip-flop.

1           8.    The differential-to-single-ended (DSE) converter as set  
2   forth in Claim 7, wherein said second NOR gate output is coupled to  
3   said reset input of said second D flip-flop via a buffer circuit.

1           9.    The differential-to-single-ended (DSE) converter as set  
2   forth in Claim 1, wherein a speed of said first comparator is  
3   determined by a biasing current of said first comparator and said  
4   biasing current is adjustable to match a frequency of said positive  
5   and negative differential input signals.

1           10.   The differential-to-single-ended (DSE) converter as set  
2   forth in Claim 1, wherein a speed of said second comparator is  
3   determined by a biasing current of said second comparator and said  
4   biasing current is adjustable to match a frequency of said positive  
5   and negative differential input signals.

1           11. A phase-locked loop (PLL) circuit comprising:  
2                 a voltage-controlled oscillator capable of receiving a  
3 control voltage and outputting a differential signal having a  
4 frequency controlled by said control voltage, said voltage-  
5 controlled oscillator comprising a ring oscillator containing a  
6 chain of delay cells having differential inputs and differential  
7 outputs;  
8                 a differential-to-single-ended (DSE) converter capable of  
9 receiving a positive differential input signal and a negative  
10 differential input signal from said voltage controlled oscillator  
11 and generating a single-ended output signal, said DSE converter  
12 comprising:  
13                     a first comparator having a non-inverting input  
14 coupled to said positive differential input signal and an  
15 inverting input coupled to said negative differential input  
16 signal;  
17                     a second comparator having an inverting input  
18 coupled to said positive differential input signal and a non-  
19 inverting input coupled to said negative differential input  
20 signal;  
21                     a first D flip-flop having an input connected to  
22 Logic 1 and clocked by a rising edge on an output of said  
23 first comparator;

24                   a second D flip-flop having an input connected to  
25       Logic 1 and clocked by a rising edge on an output of said  
26       second comparator; and

27                   a latch circuit having a first input coupled to an  
28       output of said first D flip-flop and a second input coupled to  
29       an output of said second D flip-flop, wherein a rising edge on  
30       an output of said first D flip-flop causes an output of said  
31       latch to change state and a rising edge on an output of said  
32       second D flip-flop causes said latch output to change state.

1           12. The phase-locked loop (PLL) circuit as set forth in Claim  
2       11, wherein said latch circuit comprises a first NOR gate having a  
3       first input coupled to said output of said first D flip-flop, a  
4       second input, and an output.

1           13. The phase-locked loop (PLL) circuit as set forth in Claim  
2       12, wherein said latch circuit comprises a second NOR gate having a  
3       first input coupled to said output of said second D flip-flop, a  
4       second input coupled to said first NOR gate output, and an output  
5       coupled to said second input of said first NOR gate.

1           14. The phase-locked loop (PLL) circuit as set forth in Claim  
2 13, wherein said first NOR gate is coupled to said first D flip-  
3 flop output by a first OR gate having a first input coupled to said  
4 first D flip-flop output, a second input coupled to Logic 0, and an  
5 input coupled to said first input of said first NOR gate.

1           15. The phase-locked loop (PLL) circuit as set forth in Claim  
2 14, wherein said first NOR gate output is coupled to a reset input  
3 of said first D flip-flop.

1           16. The phase-locked loop (PLL) circuit as set forth in Claim  
2 15, wherein said first NOR gate output is coupled to said reset  
3 input of said first D flip-flop via a buffer circuit.

1           17. The phase-locked loop (PLL) circuit as set forth in Claim  
2 14, wherein said second NOR gate output is coupled to a reset input  
3 of said second D flip-flop.

1           18. The phase-locked loop (PLL) circuit as set forth in Claim  
2 15, wherein said second NOR gate output is coupled to said reset  
3 input of said second D flip-flop via a buffer circuit.

1           19. The phase-locked loop (PLL) circuit as set forth in Claim  
2 11, wherein a speed of said first comparator is determined by a  
3 biasing current of said first comparator and said biasing current  
4 is adjustable to match a frequency of said positive and negative  
5 differential input signals.

1           20. The phase-locked loop (PLL) circuit as set forth in Claim  
2 11, wherein a speed of said second comparator is determined by a  
3 biasing current of said second comparator and said biasing current  
4 is adjustable to match a frequency of said positive and negative  
5 differential input signals.